**Cyclic Redundancy Check (CRC)**

**Example 1 (Without error)**

**CRC Generation at Sender side**

Original Data to be sent= 100100

Divisor (key) 1101 (x3 + x2 + 1) Polynomial function

Key length (L) = 4

Number of bits(0) to be added=L-1=4-1=3

111101

1101 100100000 (XOR operation)

1101

1000

1101

1010

1101

1110

1101

0110

0000

1100

1101

001 (Remainder)

The sender will send the original data appended with the remainder.

The transmitted data = 100100001

CRC Verification (Receiver side)

111101

1101 100100001 (XOR operation)

1101

1000

1101

1010

1101

1110

1101

0110

0000

1101

1101

000 (Remainder)

At the receiver side, if the remainder is all “0”s, it means the data is not corrupted during the transmission. (There is no error)

1001

Divisor = 100001

Number of bits (0) to be added= L-1=6-1=5

Transmitted data=100100000

100001 100100000

**Hamming Code**

**LSB (Rightmost bit)**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | - | - | - | 23 | - | - | - | 22 | - | 21 | 20 | Power of 2 |
| 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Decimal |
| 1100 | 1011 | 1010 | 1001 | 1000 | 111 | 110 | 101 | 100 | 11 | 10 | 1 | Binary |
| D12 | D11 | D10 | D9 | R8 | D7 | D6 | D5 | R4 | D3 | R2 | R1 | Data/ Redundancy |

R1 = 1

Bit position 1=1

1 AND 1= 1

Bit position 2=10

01 AND 10= 00

Bit position 3=110

001 AND 110= 000

Bit position 4= 100

001 AND 100= 000

R4 = 100 (parity position 4)

Bit position 2= 010

100 AND 010= 000 (Zero Result)

100 (AND)

010

000

Bit position 5 = 101

100 AND

101

100 (Non-zero)

Bit position 6 = 110

100 AND 110 = 100 (Non-zero Result)